

IN THE CLAIMS:

1. (Currently amended) A Schmitt trigger circuit comprising:

a first transistor coupled between a reference node and a first node, a second transistor coupled between the first node and a second node, a third transistor coupled between the second node and a third node, and a fourth transistor coupled between the third node and a power supply node, each of the first, second, third, and fourth transistors having a control terminal for receiving an input signal;

a first plurality of circuits for selectively providing a path between the first node and ~~[[a]]~~ the power supply signal node, each circuit in the first plurality of circuits comprising a ~~first~~ fifth transistor and a ~~second~~ sixth transistor, the ~~first~~ fifth transistor having a control terminal coupled to the second node and the ~~first~~ fifth transistor being coupled between the power supply signal node and the ~~second~~ sixth transistor, the ~~second~~ sixth transistor having a control terminal for receiving a control signal provided to said circuit and the ~~second~~ sixth transistor being coupled between the ~~first~~ fifth transistor and the first node, wherein each of said circuits is controlled by ~~the~~ a control signal so that only one of the first plurality of circuits provides the path between the first node and the power supply signal node at any one time;

a second plurality of circuits for selectively providing a path between the third node and ~~[[a]]~~ the reference node, each circuit in the second plurality of circuits comprising a ~~first~~ seventh transistor and a ~~second~~ an eighth transistor, the ~~first~~ seventh transistor having a control terminal coupled to the second node and the ~~first~~ seventh transistor being coupled between the reference node and the ~~second~~ eighth transistor, the ~~second~~ eighth transistor having a control terminal for receiving a control signal provided to said circuit and the ~~second~~ eighth transistor being coupled between the ~~first~~ seventh transistor and the third node, wherein each of said circuits is controlled by ~~the~~ a control signal so that only one of the second plurality of circuits provides the path between the third node and the reference node at any one time.

2. Cancelled.

3. (Previously presented) The circuit of claim 1 wherein:

the transistors in each circuit in the first plurality of circuits have a combined conductivity that is different from the combined conductivity of the transistors in any other circuit in the first plurality of circuits; and

the transistors in each circuit in the second plurality of circuits have a combined conductivity that is different from the combined conductivity of the transistors in any other circuit in the second plurality of circuits.

4. (Previously presented) The circuit of claim 1 wherein:

the first transistor, the second transistor, and the transistors in each circuit in the first plurality of circuits are of a first type; and

the third transistor, the fourth transistor, and the transistors in each circuit in the second plurality of circuits are of a second type.

5. (Original) The circuit of claim 4 wherein the transistors of the first type are n-channel metal oxide semiconductor field-effect transistors, the transistors of the second type are p-channel metal oxide semiconductor field-effect transistors, and the control terminal of each transistor is a gate terminal.

6. (Currently amended) The circuit of claim 5 wherein:

the ~~first~~ fifth transistor in each circuit in the first plurality of circuits has a different threshold voltage magnitude from that of the ~~first~~ fifth transistor in any other circuit in the first plurality of circuits; and

the ~~first~~ seventh transistor in each circuit in the second plurality of circuits has a different threshold voltage magnitude from that of the ~~first~~ seventh transistor in any other circuit in the second plurality of circuits.

7. (Currently amended) The circuit of claim 4 wherein

a source terminal of the first transistor is coupled to the reference node and a drain terminal of the first transistor is coupled to the first node;

a source terminal of the second transistor is coupled to the first node and a drain terminal of the second transistor is coupled to the second node;

a drain terminal of the third transistor is coupled to the second node and a source terminal of the third transistor is coupled to the third node;

a drain terminal of the fourth transistor is coupled to the third node and a source terminal of the fourth transistor is coupled to the power supply signal node;

in each circuit in the first plurality of circuits, a drain terminal of the ~~first~~ fifth transistor is coupled to the power supply signal node, a source terminal of the ~~first~~ fifth transistor is coupled to a drain terminal of the ~~second~~ sixth transistor, and a source terminal of the ~~second~~ sixth transistor is coupled to the first node; and

in each circuit in the second plurality of circuits, a drain terminal of the ~~first~~ seventh transistor is coupled to the reference node, a source terminal of the ~~first~~ seventh transistor is coupled to a drain terminal of the ~~second~~ eighth transistor, and a source terminal of the ~~second~~ eighth transistor is coupled to the third node.

8. (Original) The circuit of claim 1 wherein the first and second plurality of circuits each consists of first and second circuits, wherein the first circuits in each plurality of circuits receive a common control signal and the second circuits in each plurality of circuits receive a complementary version of said common control signal.

9. (Original) The circuit of claim 1 wherein the control signals provided to each circuit are programmable settings.

10. (Currently amended) A Schmitt trigger circuit comprising:

a first transistor coupled between a reference node and a first node, a second transistor coupled between the first node and a second node, a third transistor coupled between the second node and a third node, and a fourth transistor coupled between the third node and a power supply node, each of the first, second, third, and fourth transistors having a control terminal for receiving an input signal;

a plurality of first circuits for selectively providing a path between the first node and ~~[[a]]~~ the power supply signal node, each first circuit comprising a ~~first~~ fifth transistor and a ~~second~~ sixth transistor, the ~~first~~ fifth transistor having a control terminal coupled to the second node and the ~~first~~ fifth transistor being coupled between the power supply signal node and the ~~second~~ sixth transistor, the ~~second~~ sixth transistor having a control terminal for receiving a control signal provided to said circuit and the ~~second~~ sixth transistor being coupled between the ~~first~~ fifth transistor and the first node, wherein each of the first circuits is controlled by ~~the~~ a control signal so that only one of the first circuits provides the path at any one time; and

a second circuit for providing a path between the third node and ~~[[a]]~~ the reference node, the second circuit comprising a transistor having a control terminal coupled to the second node and said transistor being coupled between the reference node and the third node.

11. Cancelled.

12. (Previously presented) The circuit of claim 10 wherein:

the transistors in each of the plurality of first circuits have a combined conductivity that is different from the combined conductivity of the transistors in any other first circuit.

13. (Previously presented) The circuit of claim 10 wherein:

the first transistor, the second transistor, and the transistors in each of the plurality of first circuits are of a first type; and

the third transistor, the fourth transistor, and the transistor in the second circuit are of a second type.

14. (Original) The circuit of claim 13 wherein the transistors of the first type are n-channel metal oxide semiconductor field-effect transistors, the transistors of the second type are p-channel metal oxide semiconductor field-effect transistors, and the control terminal of each transistor is a gate terminal.

15. (Currently amended) A Schmitt trigger circuit comprising:

a first transistor coupled between a reference node and a first node, a second transistor coupled between the first node and a second node, a third transistor coupled between the second node and a third node, and a fourth transistor coupled between the third node and a power supply node, each of the first, second, third, and fourth transistors having a control terminal for receiving an input signal;

a first circuit for providing a path between the first node and ~~[[a]]~~ the power supply node, the first circuit comprising a transistor having a control terminal coupled to the second node and the transistor being coupled between the power supply node and the first node; and

a plurality of second circuits for selectively providing a path between the third node and a reference node, each circuit in the plurality of second circuits comprising a ~~first~~ fifth transistor and a ~~second~~ sixth transistor, the ~~first~~ fifth transistor having a control terminal coupled to the second node and the ~~first~~ fifth transistor being coupled between the reference node and the ~~second~~ sixth transistor, the ~~second~~ sixth transistor having a control terminal for receiving a control signal provided to said circuit and the ~~second~~ sixth transistor being coupled between the ~~first~~ fifth transistor and the third node, wherein each of the second circuits is controlled by ~~the~~ a control signal so that only one of the second circuits provides the path between the third node ~~binds~~ and the reference node at any one time.

16. Cancelled.

17. (Previously presented) The circuit of claim 15 wherein:
the transistors in each of the plurality of second circuits have a combined conductivity that is different from the combined conductivity of the transistors in any other second circuit.

18. (Previously presented) The circuit of claim 15 wherein:
the first transistor, the second transistor, and the transistor in the first circuit are of a first type; and

the third transistor, the fourth transistor, and the transistors in each of the plurality of second circuits are of a second type.

19. (Original) The circuit of claim 18 wherein the transistors of the first type are n-channel metal oxide semiconductor field-effect transistors, the transistors of the second type are p-channel metal oxide semiconductor field-effect transistors, and the control terminal of each transistor is a gate terminal.

20. (Currently amended) A Schmitt trigger circuit for receiving an input signal and outputting a signal in accordance with a voltage transfer characteristic having an upper trip point level and a lower trip point level, the circuit comprising a first plurality of independent source follower circuits, each providing a different effect on the upper trip point level when selected, and a second plurality of independent source follower circuits, each providing a different effect on the lower trip point level when selected, and wherein the Schmitt trigger circuit receives one or more control signals for selecting one source follower circuit in the first plurality of source follower circuits and one source follower circuit in the second plurality of source follower circuits so that only one source follower circuit in the first plurality of circuits and only one source follower circuit in the second plurality of circuits is selected at any one time.

21. (Original) The circuit of claim 20 wherein the circuits in the first plurality of source follower circuits comprise n-channel metal oxide semiconductor field-effect transistors, and the source follower circuits in the second plurality of circuits comprise p-channel metal oxide semiconductor field-effect transistors.

22. (Original) The circuit of claim 21 wherein:

the transistors in each circuit in the first plurality of source follower circuits have a combined conductivity that is different from the combined conductivity of the transistors in any other circuit in the first plurality of source follower circuits; and

the transistors in each circuit in the second plurality of source follower circuits have a combined conductivity that is different from the combined conductivity of the transistors in any other circuit in the second plurality of source follower circuits.

23. (Original) The circuit of claim 20 wherein the one or more control signals are programmable settings.

24. (Currently amended) A Schmitt trigger circuit for receiving an input signal and outputting a signal in accordance with a voltage transfer characteristic having an upper trip point level and a lower trip point level, the circuit comprising a plurality of independent source follower circuits each providing, when selected, a different effect on one of the upper trip point level and the lower trip point level, and wherein the Schmitt trigger circuit receives one or more control signals for selecting one source follower circuit in the plurality of source follower circuits so that only one source follower circuit is selected at any one time.

25. (Previously presented) A method of providing an adjustable hysteresis characteristic in a Schmitt trigger circuit comprising:

providing one or more control signals to the Schmitt trigger circuit; and

in response to the one or more control signals, selecting one of a first plurality of independent parallel source follower circuits to provide a first desired signal path in the Schmitt trigger circuit.

26. (Previously presented) The method of claim 25 further comprising:

in response to the one or more control signals, selecting one of a second plurality of independent parallel source follower circuits to provide a second desired signal path in the Schmitt trigger circuit.

27. (Original) The method of claim 25 comprising providing the one or more control signals based on the voltage level of a power supply signal in the Schmitt trigger circuit.

28. (Original) The method of claim 25 comprising programmably providing the one or more control signals .